EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	("20040084701").PN.	US-PGPUB; USPAT	OR	OFF	2006/04/26 16:01
L2	0	(amorphous with ferroelectric) and (insulative or insulating or insulator or dielectric) and (anneal or annealing or (heat adj treatment) or (heat adj treated) or (heat adj treating)) and (ferroelectric with (crystalization or crystalizing or crystalized))	US-PGPUB; USPAT	OR	ON	2006/04/26 16:10
L3	1	(amorphous with ferroelectric) and (insulative or insulating or insulator or dielectric) and (anneal or annealing or (heat adj treatment) or (heat adj treated) or (heat adj treating)) and (ferroelectric with (crystalization or crystalizing or crystalized))	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/26 16:10
L4	1	(ferroelectric near5 capacitor) and (anneal or annealing or (heat adj treatment) or (heat adj treated) or (heat adj treating)) and (ferroelectric with (crystalization or crystalizing or crystalized))	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/26 16:11
L5	1	(ferroelectric near5 capacitor) and (anneal or annealing or (heat adj treatment) or (heat adj treated) or (heat adj treating)) and (ferroelectric with (crystalization or crystalizing or crystalized))	US-PGPUB; USPAT	OR	ON	2006/04/26 16:12
L6	0	(ferromagnetic near5 capacitor) and (anneal or annealing or (heat adj treatment) or (heat adj treated) or (heat adj treating)) and (ferroelectric with (crystalization or crystalizing or crystalized))	US-PGPUB; USPAT	OR	ON	2006/04/26 16:12
L7	0	(ferromagnetic near5 capacitor) and (ferroelectric with (crystalization or crystalizing or crystalized))	US-PGPUB; USPAT	OR	ON	2006/04/26 16:12
L8	0	(ferromagnetic near5 capacitor) and (crystalization or crystalizing or crystalized)	US-PGPUB; USPAT	OR	ON	2006/04/26 16:13
L9	0	(ferromagnetic near5 capacitor) and (crystalization or crystalizing or crystalized)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/26 16:13

DOCUMENT-IDENTIFIER: US 20020168785 A1

TITLE: Ferroelectric composite material, method of making same, and memory utilizing same

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Abstract Paragraph - ABTX (1):

A ferroelectric memory includes a plurality of memory cells each containing a ferroelectric thin film including a microscopically composite material having a ferroelectric material component and a fluxor material component, the fluxor material being a different chemical compound than the ferroelectric material. The fluxor is a material having a higher crystallization velocity than the ferroelectric material. The addition of the fluxor permits a **ferroelectric** thin film to be **crystalized** at a temperature of between 400.degree. C. and 550.degree. C.

Detail Description Paragraph - DETX (11):

[0027] The layered superlattice materials do not include every material that can be fit into Formula (1), but only those ingredients which spontaneously form themselves into a layer of distinct crystalline layers during crystallization. This spontaneous crystallization is typically assisted by thermally treating or **annealing** the mixture of ingredients. The enhanced temperature facilitates self-ordering of the superlattice-forming moieties into thermodynamically favored structures, such as perovskite-like octahedra. The term "superlattice generator elements" as applied to S1, S2 . . . Sk, refers to the fact that these metals are particularly stable in the form of a concentrated metal oxide layer interposed between two perovskite-like layers, as opposed to a uniform random distribution of superlattice generator metals throughout the mixed layered superlattice material. In particular, bismuth has an ionic radius that permits it to function as either an A-site material or a superlattice generator, but bismuth, if present in amounts less than a threshold stoichiometric proportion, will spontaneously concentrate as a non-perovskite-like bismuth oxide layer.

Detail Description Paragraph - DETX (35):

[0045] Another ferroelectric memory architecture in which a ferroelectric memory device according to the invention can be used is shown in FIG. 4. This is sometimes referred to as a linked cell structure. The basic memory cell 82 consists of one switch 80 which preferably is a MOSFET transistor 80, in

parallel with a **ferroelectric capacitor** 81. FIG. 4 shows a 3.times.1 linked cell structure, which can be considered as a one-column array 99. Transistor 80 and **ferroelectric capacitor** 81 form cell 82; transistor 83 and **ferroelectric capacitor** 84 form a second cell 85; transistor 86 and **ferroelectric capacitor** 87 form a third cell 88. The three cells 82, 85 and 88 form a column of memory cells. Transistor 89 is a transistor used for reading. Transistor 91 controls whether the Reset signal is applied to node 92 or not. Transistor 92 control whether Set signal is applied to node 95 or not. The above three transistors, 90, 91, and 94, are the control transistors, which can all be replaced by other more complicated circuits to improve the performance. That is, they can be considered as part of the peripheral circuit. An actual ferroelectric memory utilizing this architecture will normally have more than three linked cells in a column and will have many columns of cells.

Detail Description Paragraph - DETX (36):

[0046] FIG. 5 shows a cross-sectional view of a portion of another exemplary nonvolatile integrated circuit ferroelectric memory 100 that can be fabricated according to the invention. The general manufacturing steps for fabricating such integrated circuits containing MOSFETs and **ferroelectric capacitor** elements are described in Mihara, U.S. Pat. No. 5,466,629 and Yoshimori, U.S. Pat. No. 5,468,684, which are hereby incorporated by reference as if fully disclosed herein. General fabrication methods have been described in other references also. Therefore, the elements of the circuit of FIG. 5 will be simply identified here.

Detail Description Paragraph - DETX (39):

[0049] As depicted in FIG. 5, a bottom electrode layer 122, preferably made of platinum and having a thickness of 90 nm, is deposited on diffusion barrier layer 121. Then a ferroelectric thin film 124 is formed on bottom electrode layer 122. According to the invention, the ferroelectric thin film 124 is a composite material and is preferably 80 nanometers (nm) or less thick. Most preferably, it is 50 nanometers or less. A top electrode layer 126, preferably made of platinum and having a thickness of 90 nm, is formed on the ferroelectric thin film 124. Bottom electrode layer 122, ferroelectric thin film 124 and top electrode layer 126 together form **ferroelectric capacitor** 128. The method of formation of ferroelectric film 124 is discussed in detail below.

Detail Description Paragraph - DETX (40):

[0050] Wafer substrate 102 may comprise silicon, gallium arsenide or other semiconductor, or an insulator, such as silicon dioxide, glass or magnesium oxide (MgO). The bottom and top electrodes of **ferroelectric capacitors** conventionally contain platinum. It is preferable that the bottom electrode

contains a non-oxidized precious metal such as platinum, palladium, silver, and gold. In addition to the precious metal, metal such as aluminum, aluminum alloy, aluminum silicon, aluminum nickel, nickel alloy, copper alloy, and aluminum copper may be used for electrodes of a ferroelectric memory. Adhesive layers (not shown), such as titanium, enhance the adhesion of the electrodes to adjacent underlying or overlying layers of the circuits.

Detail Description Paragraph - DETX (41):

[0051] A second interlayer dielectric layer (ILD) 136 made of NSG (nondoped silicate glass) is deposited to cover ILD 116, diffusion barrier layer 121, and **ferroelectric capacitor** 128. A PSG (phospho-silicate glass) film or a BPSG (boron phospho-silicate glass) film could also be used in layer 136.

Detail Description Paragraph - DETX (48):

[0058] Memory cell array 445 contains 128.times.128=16,384 memory cells, which is conventionally designated as 16K. These cells are **ferroelectric switching capacitor**-based cells such as 73, 82, or 100. Lines 446 correspond to the word lines, such as 36. Lines 447 correspond to the gate and bit lines, such as 32 and 34.

Detail Description Paragraph - DETX (53):

[0063] In parallel with either the combined precursor formation step 360 or the solvent and concentration control step 383, the substrate 14, 53, 122 is prepared. If the substrate is a metallized substrate, such as the substrate 14, then the substrate is provided in step 384A by forming the layers 12, 13, and 14 and is then prebaked in step 386A. If the substrate is a non-metallized substrate, such as a silicon or gallium arsenide single crystal, the substrate is provided in step 384B and dehydrated in step 386B. In step 387 the substrate is coated with the precursor. In the examples discussed below, the coating was done by a spin-on process, though a process such as a misted deposition process as described in U.S. Pat. No. 5,540,772, which is hereby incorporated by reference, or dipping or other suitable coating process may be used. The coated substrate is then dried in step 388, and then baked in an RTP (rapid thermal processor) unit. If the desired thickness of the layer 15, 55, 124 is not obtained, then the series of coat, dry, and RTP bake steps 87, 88, and 89 are repeated as many times as required to build up the desired thickness. However, in the preferred embodiment, only one layer is formed. The wafer 10, 40, 100 is then annealed in step 392, the top electrode 16, 126, or gate 58 is deposited in step 93 by sputtering or other suitable process, and the wafer is then, optionally, annealed again in step 394. The capacitor 17, 128 or gate structure 50 is then structured by ion milling, chemical etching, or other suitable process in step 395. Then follows, in step 396, a second

"second **anneal**" step, which will be the third **anneal** if step 394 was done. This completes the process if a capacitor device as in FIG. 1 is the desired end result; however, in the case of an integrated circuit as in FIGS. 3-5, there follows completion steps 397 such as contact metallization, capping, etc. As will be discussed further below, not all of the steps outlined above are necessary for every device; some steps are optional and others are used only for certain materials.

Detail Description Paragraph - DETX (61):

[0071] Once the desired film thickness has been obtained, the dried and preferably baked film is annealed in step 392, which is referred to as a first **anneal** to distinguish it from subsequent **anneals**. The first **anneal** is preferably performed in an oxygen atmosphere in a furnace. The oxygen concentration is preferably 20% to 100%, and the temperature is between 400.degree. C. and 600.degree. C., and preferably 550.degree. C. or lower. The numerous nuclei, small grains generated by the RTP bake step, grow, and a well-crystallized ferroelectric film is formed under the oxygen-rich atmosphere.

Detail Description Paragraph - DETX (62):

[0072] After the first **anneal,** the second or top electrode 16, 126 or the gate electrode 58 is formed. Preferably, the electrode is formed by RF sputtering of a platinum single layer, but it also may be formed by DC sputtering, ion beam sputtering, vacuum deposition or other appropriate deposition process. If desirable for the electronic device design, before the metal deposition, the composite material 15 may be patterned using conventional photolithography and etching, and the electrode 16, 126, 58 is then patterned in a second process after deposition.

Detail Description Paragraph - DETX (63):

[0073] The wafer 10, 40, 100 including the composite 15, 55, 124 covered by electrode 16, 58, 126 may be annealed before the patterning step 95 described above in a **heat treatment** designated in FIG. 7 as the second **anneal** (1) step 394, after the patterning step 395 by a **heat treatment** designated in FIG. 7 as the second **anneal** (2) step 396, or both before and after the patterning step 395. The second **anneal** is preferably performed in an electric furnace at a temperature between 400.degree. C. and 600.degree. C., preferably, 550.degree. C. or less.

Detail Description Paragraph - DETX (64):

[0074] The second **anneal** releases the internal stress in the top electrode 16, 58, 124 and in the interface between the electrode 15, 58, 124 and the

composite material 15, 55, 124. At the same time, the second **annealing** step 394 or 396 reconstructs microstructure in the composite resulting from the sputtering of the top electrode, and as a result improves the properties of the material.

Detail Description Paragraph - DETX (67):

[0077] As another example, precursors were formed as discussed above for 50%/50% composite of a PbO/GeO.sub.2 fluxor with a strontium bismuth tantalate ferroelectric, which produced a ferroelectric composite material having a polarizability of about 7 microcoulombs/cm.sup.2 at an **anneal** temperature of 500.degree. C. Other fluxors combined with either strontium bismuth tantalate or strontium bismuth niobium tantalate were GeO.sub.2, B.sub.2O.sub.3, BaO/2B.sub.2O.sub.3, PbO/2B.sub.2O.sub.3 and B.sub.2O.sub.3/GeO.sub.2 It was found that the ratio of fluxor to ferroelectric could be varied from about 20%/80% ratio to about 80%/20% ratio and still get useable composite materials.

Detail Description Paragraph - DETX (68):

[0078] A feature of the invention is that by combining a precursor for a material that has a crystal growth velocity that is higher than the crystal growth velocity of a basic ferroelectric material with a precursor for the ferroelectric material, the ferroelectric material can be formed at a much lower crystallization temperature than without the fluxor. It is a feature of the invention that the thermal budget for drying, baking and **annealing** the ferroelectric thin film is much smaller than the thermal budget for prior art ferroelectric thin films.

Claims Text - CLTX (11):

10. A ferroelectric memory as in claim 1 wherein said **ferroelectric device is a ferroelectric capacitor**.

Claims Text - CLTX (12):

11. A **ferroelectric memory as in claim 10 wherein said ferroelectric capacitor** is a stacked capacitor.

Claims Text - CLTX (30):

29. A ferroelectric memory as in claim 20 wherein said **ferroelectric device is a ferroelectric capacitor**.

Claims Text - CLTX (31):

30. A **ferroelectric memory as in claim 29 wherein said ferroelectric capacitor** is a stacked capacitor.